Why shall (or should not) eight-Slot CPCI Backplanes terminated?

CPCI system simulation has shown that when using a PCI buffer showing strongest drive characteristic (refer to the PCI specification V-I curves) in combination with a lightly loaded eight-slot backplane configuration, the 10 ns maximum propagation delay for PCI signals can be violated by stronger over- and undershot.
Lightly loaded is understand by loaded System Slot only and its adjacent Peripheral Slot, all other Slots of higher numbers are empty. Only two boards are plugged into the backplane.

For this very specific system configuration, fast Schottky diode signal termination shall be added to the end of the backplane furthest from the System Slot on all bussed PCI signals, as illustrated in Figure 3 of PICMG 2.0 R3.0 Specification.

The possible violation of propagation delay is only detected by simulations, not in practical cases. Also, in practise, this very specific configuration that in a 8 Slot system only the System Slot and the adjacent one is loaded, is very seldom met. Further, PCI buffer run more at "typical" drive strength than with "strongest" drive strength.

If only during system integration the Backplane may loaded only with the System Controller board an a Peripheral board, the Peripheral board should be plugged into any other Slot than the Slot adjacent to the System Slot. In this case, the possible timing violation due to stronger over-/undershoot is in a very efficient and easy way avoided.

Plugging the Peripheral board into a Slot of higher number, the propagating signal is more smoothed, which reduces over- and undershot. But the main advantage by zero investment for no additional components is the reduced propagation delay by a reduced signal traffic path.