Technical Data
Schroff PXI - Backplanes

part# 23006 – 57n & 58n

Mechanical and Climatic Parameters	**Standard**	**on request**
Operating Temperature	0°C - +70°C	
Storage Temperature	-55°C - +105°C	
Humidity conformal coating	max 95%, not condensing	 on request
Flammability: • PCB, Connectors • Ceramic caps	 UL 94 V-0 fire-proof	
Connectors • Performance level per IEC 61076-4-101 • Mechanical Durability (Mating Cycles) • Total Insertion and Extraction Force (mating)	IEC 61076-4-101 (HardMetric 2mm Grid) level 2 > 250 cycles < 0,7 N / Pin	 level 1 > 500 cycles
Vibration acc. DIN 41640 Part 15	10Hz – 500Hz 5g rms	5Hz – 2000Hz 20g rms
Shock (10 pulses each direction x,y,z)	10g, 6ms	
Low Pressure / Altitude (if max Board voltage per single isolation gap doesn't exceed 12V)	no restrictions	
Construction:	12 - Layer Stripline	
Dimensions (mm) • Width (pl. see Dwg.) • Height 3U / 6U • Thickness	 20,32mm x # Slots-1mm 128,7mm / 262,05 mm 3,9 mm +/- 0,2 mm	

Electrical Parameters:

Specifications	PICMG 2.0 R3.0 PICMG 2.1 PICMG 2.6 PICMG 2.8 PICMG 2.9 PICMG 2.10 PXI Spec	CPCI Core Specification CPCI Hot Swap Specification Bridging Specification Pin Registration for PXI System Management Bus Spec. Keying Specification PXI Specification Rev. 2.0
Service Life: MTBF, acc. to MIL HDBK 217F, cond.: 25°C, ground, benign 3U 8-Slot	 more than 600.000h	
Characteristic Impedance PCI Bus PXI Local Bus	 65 Ω ± 10 % 75 Ω ± 10 %	
Ohmic Resistance of Signal Tracks PCI Bus PXI Local Bus	 < 80mΩ/Slot < 90mΩ/Slot	
Hot Swap	supported	

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Electrical Parameters (II):

Termination (only 8 Slot Backplanes)	Schottky diodes (on request), plugable termination board
Power input	• Power bugs for wiring or • special Adapter Board to use an ATX cable; this board can act as a power distribution star point within the Systems
max. Current Carrying Capacity • 5V/GND • 3,3V/GND	 10 A per Slot 10 A per Slot
max. Voltage Drop on +5V or +3,3V	< 40mV
VI/O • bridging (default) • on request	+5V (default), blue key; 3,3V optional (yellow key) • field changeable, using M4 screws and a bus bar • fixed during bp assy by using a Power Bug cable loop using Faston crimp contacts
PCI Clock frequency	33 MHz (66MHz up to 5 Slots)
PCI Bus Width	64bit
Data Transfer Rate (peak) • 33 MHz • 66 MHz	 132 Mbyte/s (32 bit) / 264 Mbyte/s (64 bit) 264 Mbyte/s (32 bit) / 528 Mbyte/s (64 bit)
Bridging of Backplanes clock frequency: primary / secondary • 33 MHz / 33MHz • 66 MHz / 33MHz • 66 MHz / 66MHz	Backplanes of slot numbers equal or higher than 4 up to 7 Slots can be bridged primary / secondary • any slot number as primary and secondary b/p • 4 Slots / any Slot number • 4 Slot / 4 Slot
PXI Clock • accuracy • switching between external and internal sources, ◆ min Pulse width: ◆ min time between successive edges of the same polarity:	10 MHz skew: < 0,5ns; <1,0ns for segmented Backplanes Jitter: < 0,2ns > 30ns > 80ns