

PRODUCT BRIEF

Pigeon Point BMR-STM32-ATCA Reference Design

Board Management for IPMCs

Within AdvancedTCA® and Custom Derivative Architectures

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The BMR-STM32-ATCA design is one of a series of Pigeon Point Board Management Reference (BMR) designs. This member of the series provides an IPM Controller (IPMC) for AdvancedTCA and custom derivative architectures, based on the STM32F407 32-bit microcontroller from STMicroelectronics.

This reference design is delivered in a Pigeon Point Board Management Starter Kit (which is detailed in a separate Product Brief).

The kit includes:

- An STM32F407 microcontroller design that implements the core of an IPMC, working with the ARM Cortex-M4 processor and supporting peripherals. This design is ready to be adapted for your board or other intelligent Field Replaceable Unit (FRU).
- Schematics for a corresponding IPMC subsystem, ready for integration into the schematic for your board, with adaptation as necessary
- Firmware for that subsystem, delivered in source form and with development tools—ready for simple and quick adaptation to your requirements
- One-stop support from nVent SCHROFF experts for schematics, firmware and software used in developing and delivering your Pigeon Point BMR-based IPMC

The photo in the left column shows the core of a BMR-STM32-ATCA IPMC. The active components are:

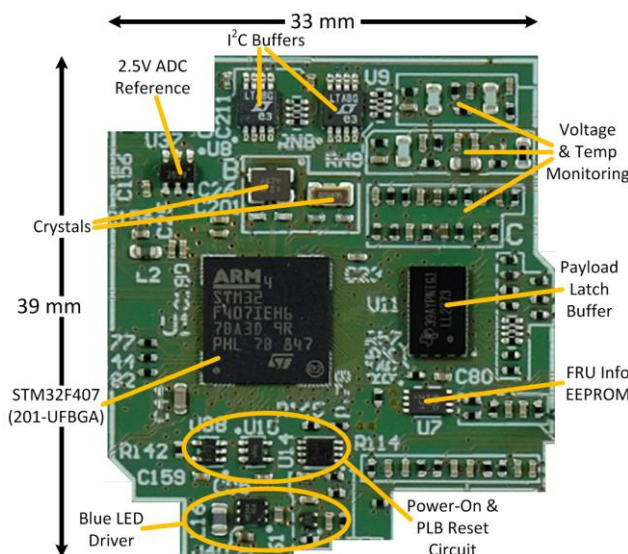
- The STM32F407 Microcontroller
- Dual IPMB buffers to isolate the IPMC from the dual redundant IPMB-0 implemented on the backplane
- An external 12MHz crystal to provide the operating frequency and an external 32.768 kHz oscillator for the internal RTC and watchdog timer functions.

Specification compliant and interoperability tested

- PICMG 3.0 R3.0 as amended by ECN 3.0-3.0-001, the AdvancedTCA base specification, plus HPM.1 R1.0, the Firmware Upgrade specification
- HPM.2 and HPM.3, the LAN-attached IPM Controller and DHCP-assigned Platform Management Parameters specifications (revisions R1.1 and R2.0, respectively)
- IPMI v1.5, document revision 1.1 and the relevant subset of IPMI v2.0, document revision 1.0, plus relevant errata
- PICMG 3.0, HPM.2/3 and IPMI 2.0 compliance includes support for Internet Protocol version 6 (IPv6)
- Thoroughly tested with other management components at PICMG TCA-IWs (Interoperability Workshops)

Highly adaptable, including for custom, derivative management architectures

- Usable for blades in bladed systems or for main system boards in non-bladed systems, such as appliances
- Independent of number, size and physical form factors of boards
- Board hot swap support available, but need not be used
- Interface to higher level management can be based on either I²C or Ethernet, among other options
- Allows integration of standards-based boards with proprietary architecture boards within a single bladed system, if desired



Full support for core hardware requirements

- 32-bit Cortex operating at 168 MHz for IPMC firmware execution
- IPMI-aware voltage and temperature monitoring via designated STM32F407 ADC sensors
- Payload voltage monitoring (including 48V supply)
- Direct LAN attachment interface or sideband LAN attachment interface implemented via Network Controller Sideband Interface (NC-SI), capable of handling IPMI over LAN (including Serial over LAN, HPM.1 upgrades, IPMB trace access and other HPM.2-compliant extensions)
- HPM.2-compliant extended inactive state management, including extended management power support
- ATCA hot swap interfaces (handle and blue LED)
- Dual redundant IPMB-0
- Hardware address detection from backplane
- FRU LED management
- Payload power supply controls (multiple voltage levels) using PMBus or control GPIOs, with optional persistence across IPMC resets
- Control of E-Keying governed fabric interfaces
- Optional persistence of above controls across IPMC resets
- Optional local System Event Log (SEL)
- Optional infrastructure for non-intelligent Rear Transition Modules
- UART-based payload interface
- UART-based serial debug interface

Optional support for special purpose functionality

- Telco (dry contact) alarm management, including choice of IPMI interfaces: ATCA-defined or Pigeon Point specific
- Shelf FRU information SEEPROM access

Small footprint

- Core IPMC can fit in the following package-dependent footprint: 33 mm x 39 mm (UFBGA176+25)

Comprehensive, readily adaptable firmware

- All mandatory and many optional IPMI/ATCA commands supported over the backplane IPMB-0

- Numerous Pigeon Point extension commands, primarily used over the payload and serial debug interfaces
- Payload alert notifications over payload interface for sensor events and receipt of reset/shutdown commands
- PICMG HPM.1 firmware upgrade support
- Simple—but highly flexible—configuration of firmware features

Sophisticated, HPM.1-compliant support for firmware upgrades

- Firmware upgrades over any IPMI interface to the IPMC, with redundant copies and automatic fallback after failed upgrade
- IPMC is fully functional during upgrade
- Bootloader can be upgraded without using JTAG
- Framework for managing firmware upgrades that include changes in data structures that are preserved across IPMC resets to eliminate disruptive upgrades
- IPMC FRU Information implemented as additional HPM.1 component, allowing FRU Information upgrades independently of firmware
- Optional upgrades via IPMI over LAN interface
- Open source ipmitool supplied as upgrade agent
- HPM.1 compliance means that any compliant upgrade agent can upgrade any compliant IPMC

Optional support for non-intelligent Rear Transition Modules (RTM)

- Includes specific hardware/firmware support for interface between front board and RTM
- Assumes no management controller on RTM; RTMs equipped with Module Management Controller cannot be supported with the BMR-STM32-ATCA reference design. The BMR-A2F-AMCc product (see separate product brief) can be used to support intelligent RTMs
- Allows compliance with ATCA requirements regarding how an RTM is represented by the IPMC

Choice of serial interface protocols (SIPL variants) supported via UARTs to payload processor and serial debug interface

- SIPL-TM, based on IPMI-defined Terminal Mode of the Serial/Modem Interface,
- SIPL-BM based on IPMI-defined Basic Mode,
- Either protocol selectable individually for either serial interface
- SIPL-TM: human-oriented and ASCII-based, intended primarily for the serial debug interface
- SIPL-BM: machine-oriented and binary-based, intended primarily for the UART-based payload interface
- Both protocols use encoded forms of raw IPMI messages, which are handled by the IPMC essentially like IPMB messages

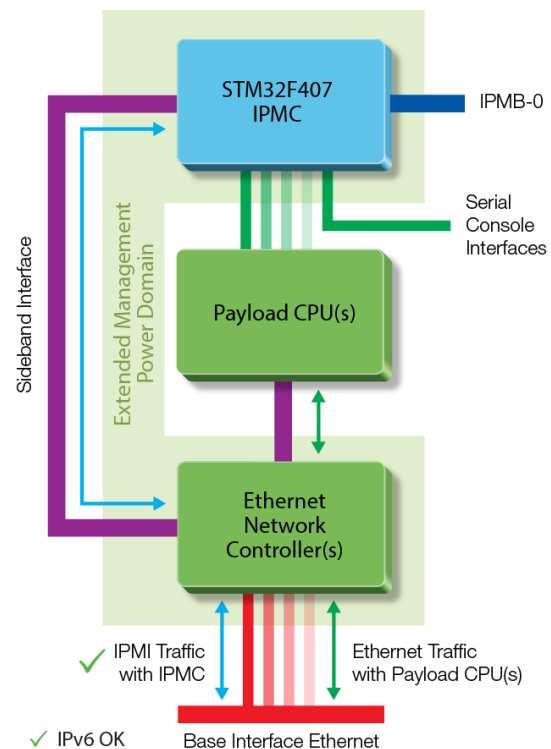
Optional Simple Network Stack

- Ethernet layer, including drivers for STM32F407 Ethernet MAC
- Internet Protocol (IP) layer, which cooperates with ARP module to resolve IP address to MAC addresses
- IP-based protocol layer, including UDP and ICMP
- Provides foundation for application protocols, such as RMCP and RMCP+

Optional HPM.2 IPMI over LAN

- Primary client of simple network stack
- IPMI 2.0 compliant implementation of extended Remote Management Control Protocol (RMCP+), including session establishment
- RMCP+ compliant authentication, integrity and confidentiality, specifically via the following algorithms (all using IPMI 2.0-compliant random number generation):
 - Authentication: HMAC-SHA1
 - Integrity: HMAC-SHA1-96
 - Confidentiality: AES-CBC-128
- IPMI over LAN and SoL payload types in RMCP+, with framework for supporting further payload types
- Enables HPM.1 firmware upgrades and HPM.2 IPMI trace collection via LAN channel

- Optional HPM.3 IPv4 or IPv6 parameter assignment via direct interaction with DHCPv4 or DHCPv6 server or by Shelf Manager¹ or other proxy
- Supported LAN interfaces with STM32F407 RMII-equipped Ethernet MAC include:
 - NC-SI², tested with selected Intel NCs
 - Direct Ethernet, where the LAN connection is dedicated to management traffic, not shared with the payload



¹ The Pigeon Point Shelf Manager can be configured to assign IPv4 address parameters to LAN-attached IPMCs via HPM.3-defined mechanisms.

² NC-SI is an open specification published by the Distributed Management Task Force (DMTF, www.dmtf.org) that uses the Reduced Media Independent Interface (RMII) as the physical transport between the network and management controllers.

Optional support for HPM.2 extended inactive state management and extended management power

- Extended inactive state management support, enables LAN attach facilities (including IPMI over LAN, Serial over LAN and IPMI trace collection) to operate even when IPMC-managed FRU is not active (e.g., set up and enabled before payload is powered for first time), greatly increasing diagnostic visibility benefits
- Extended management power support can be implemented in an IPMC if LAN attach configuration requires more than specification-defined 15 W management power.
- Shelf Manager queries IPMC for extended management power needs
- If needed, Shelf Manager allocates additional power for IPMC, separate from payload power
- Example need scenario: extended management power domain (IPMC plus LAN attach Ethernet controller) requires > 15 W of power

Optional HPM.2 Serial over LAN (SoL)

- Uses HPM.2 IPMI over LAN facility to support Serial over LAN via NC-SI or a direct Ethernet connection
 - Payload SoL requires separate physical UART connection between payload and IPMC
 - SoL for IPMC serial debug interface available, also
 - HPM.2 SOL extensions allow up to 15 concurrent SOL sessions, each with specific serial ports accessible to the IPMC, user chosen from up to 255 physical on-board serial ports
- Supplied open source ipmitool can be used as SoL client

Optional local System Event Log (SEL)

- Requires SEEPROM storage on board
- IPMI compliant System Event Log for events generated on the FRU(s) represented by the IPMC
- Can provide a useful historical record of events that have been recorded during operation of a board, perhaps for use in board diagnosis at a maintenance depot
- Events are also forwarded to Shelf Manager, as required by ATCA

Optional support for persistent modifications to Sensor Data Records

- Non-volatile copy of SDR Repository can be configured in on-board SEEPROM
- Sensor threshold and hysteresis values can be configured dynamically via extension commands, and are thereafter persistent across power cycles and resets of the board

Optional support for payload-controlled sensors

- Allows sensors that are implemented by the payload (e.g. an I²C sensor connected to the payload CPU) but exposed by the IPMC as its own
- Covers discrete and threshold sensors

Optional support for persistent configuration parameters

- Parameters preserve values across IPMC power cycles and resets
- Used for most persistent data, such as serial port parameters, LAN and SoL parameters
- Framework for such treatment of other parameters, including those in custom firmware extensions

Simple, but powerful, firmware configuration mechanisms

- Configuration variables in a single config.h source file parameterize and determine inclusion/exclusion of subsystems during firmware image build
- Binary configuration files for FRU Information and Sensor Data Records (SDR) merged into firmware image
- FRU Information and SDR files produced from textual representations by special supplied compilers

Comprehensive Cortex-M4 development environment

- Linux- or Windows-based cross GNU C compiler and binary utilities for Cortex-M4 processor (available for download from a third-party web site)
- GNU MCU Eclipse support
- JTAG-based firmware download using ST-LINK JTAG programmer from STMicroelectronics

Numerous extensions beyond required IPMI/ATCA/HPM.1 commands and functionality

- Cold Reset
- Warm Reset
- Get Device GUID
- Get System GUID
- Set User Name
- Activate/Deactivate Payload
- Suspend/Resume Payload Encryption
- Get Payload Activation Status
- Get Payload Instance Info
- Get/Set User Payload Access
- Get Channel Payload Support
- Get Channel Payload Version
- Get Channel OEM Payload Info Command
- Get/Set SOL Configuration Parameters
- Get/Set Sensor Hysteresis
- Get/Set Sensor Thresholds
- Get/Set Sensor Event Enable
- Re-arm Sensor Events
- Get Sensor Event Status
- Get Sensor Type
- Get/Set Fan Level
- Get IPMB Link Info
- Get Telco Alarm Capability
- Get/Set Telco Alarm State
- Abort Firmware Upgrade
- Query Self-test Results
- Query Rollback Status
- Initiate Manual Rollback
- Graceful Reboot and Issue Diagnostic Interrupt options in FRU Control command
- Get/Set FRU LED State commands for blue LED
- Lamp Test function of Set FRU LED State command

Rich set of Pigeon Point extension commands

- All extension commands implemented as IPMI-compliant OEM messages
- Get Status
- Get/Set Serial Interface Properties
- Get/Set Debug Level
- Get/Set Hardware Address
- Get/Set Handle Switch
- Get/Set Payload Communication Timeout
- Disable/Enable Payload Control
- Reset IPMC
- Hang IPMC³
- Bused Resource Control/Status
- Graceful Reset
- Diagnostic Interrupt Results
- Set/Clear Telco Alarm
- Get Telco Alarm Sensor Number
- Get/Set Payload Shutdown Timeout
- Get/Set Local FRU LED State
- Update Discrete Sensor
- Update Threshold Sensor
- Set EEPROM SDR Data
- Set EEPROM SDR Hysteresis
- Set EEPROM SDR Thresholds
- Reset EEPROM SDR Repository
- Get/Set GPIO Signal State
- Reset Non-Volatile Parameters and Reboot
- Get/Set FRU Info Write-Protect State

Reference Implementation

A bench top implementation called the BMR-STM32-IPMC-BTR is shown on the next page. In addition to the BMR-STM32-ATCA IPMC core, the board includes implementations of the optional IPMC features and numerous LEDs, switches and headers to allow lab experimentation with the behavior of the IPMC. Below the photo is a block diagram of a BMR-STM32-ATCA IPMC.

³ This function is used to test the IPMC watchdog.

